(12) UK Patent Application (19) GB (11) 2 297 652 (13) A

(43) Date of A Publication 07.08.1996

(21) Application No 9601609.2

(22) Date of Filing 26.01.1996

(30) Priority Data
(31) 9502178 (32) 03.02.1995 (33) GB

(71) Applicant(s)
Plessey Semiconductors Limited

(Incorporated in the United Kingdom)

Cheney Manor, SWINDON, Wiltshire, SN2 2QW, United Kingdom

(72) Inventor(s)
David John Pedder

(74) Agent and/or Address for Service
Maurice Edward Casey
GEC Patent Department, Waterhouse Lane, CHELMSFORD, Essex, CM1 2QX, United Kingdom

(51) INT CL[6]
H05K 1/18 , H01L 23/488 , H05K 3/34

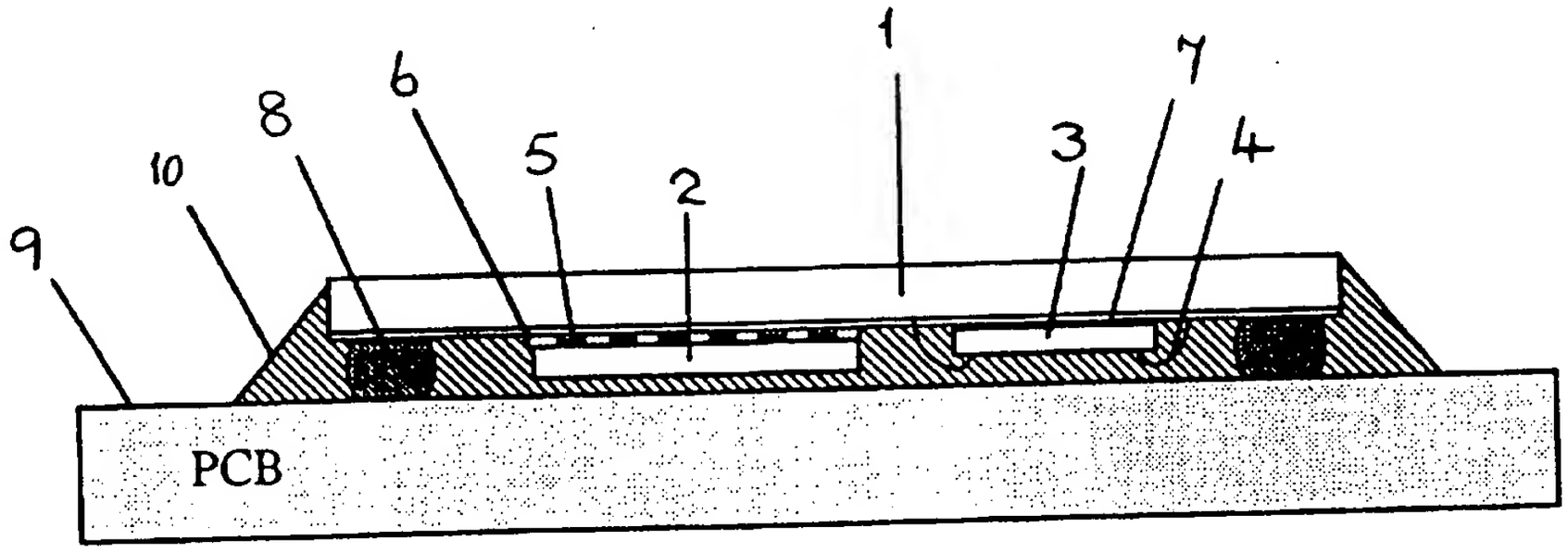
(52) UK CL (Edition O)
H1R RAB
H1K KRG K1FJ K1FL K1FX K4C8 K4F11G K4F7A K4F9 K5A1 K5A5 K5D2 K5D9 K5N

(56) Documents Cited
GB 1137907 A **US 4710798 A**

(58) Field of Search
UK CL (Edition O) **H1K KRG KRX , H1R RAA RAB**
INT CL[6] **H01L , H05K**
Online:WPI

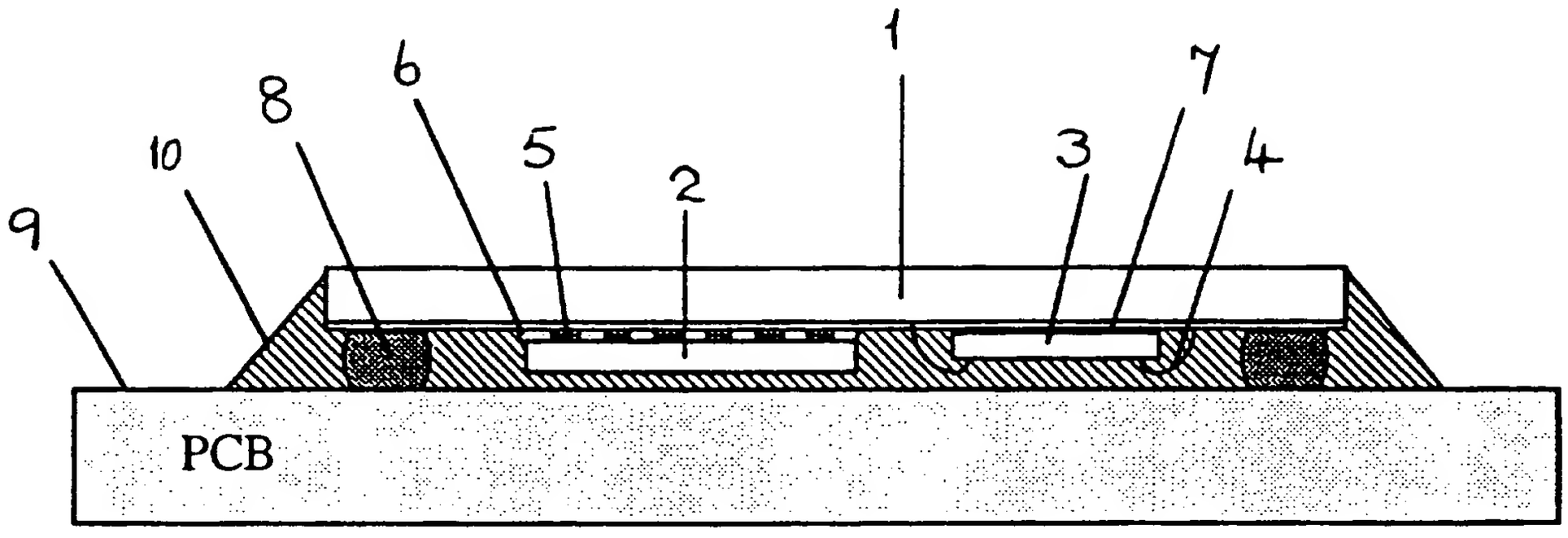
(54) Microchip module assemblies

(57) Low profile microchip module assemblies are formed by first mounting one or more active semiconductor integrated circuit chips 2,3 on a multilayer metallisation and dielectric structure on a substrate 1 of, say, silicon or alumina, by wire bonding or flip-chip solder bonding, and then inverting the substrate and mounting it on a printed circuit board 9 by means of solder bump connections 8. The solder bump connections are sufficiently high for the chips to be held clear of the printed circuit board.



GB 2 297 652 A

1/1



Microchip Module Assemblies

The present invention relates to microchip module (MCM) assemblies.

Modern microelectronic system construction is demanding ever greater levels of integration and the use of packaging techniques that provide cost effective, compact assemblies and sub-assemblies. The demand is particularly strong in the area of portable electronic products where assembly size, weight, power consumption and cost are critical. The emergence of the PCMCIA computer industry standard for miniaturised circuit card expansion slots in portable computing equipment also places a growing emphasis on the physical height of electronic assemblies.

A variety of thin film deposited technologies, known as MCM-D, have been developed to provide islands of high density integration in such electronics assemblies. The MCM-D assemblies involve multiple silicon, GaAs and related active devices mounted on the MCM-D substrate by wire bonding or by flip chip solder bonding. The MCM-D substrate provides a multilayer metallisation and dielectric structure defined on a silicon, alumina or other suitable base substrate layer to provide ground, power and signal routing structures and, in certain MCM-D processes, a full range of integrated thin film passive components, including resistors, capacitors and inductors. The substrate is manufactured by IC-like processing methods and employs feature sizes that are between those of standard IC and pcb processes.

A variety of techniques may be employed for packaging MCM-D assemblies. High reliability, high thermal dissipation MCM-D designs may be packaged in hermetic ceramic enclosures manufactured by established methods. Module designs that require an hermetic environment for reasons of device performance stability, for example where SAW devices are included within the package structure, may also employ ceramic packaging techniques. The package form factor will be selected according to the application and may include leadless ceramic chip carriers, leaded ceramic flatpacks, pin grid arrays, land grid arrays and ball grid arrays.

Plastic packaging techniques may also be employed with MCM-D assemblies. Substrate assemblies may be mounted on metallic lead frames, wire bonds made between the substrate and the lead frame and the plastic package body defined by

injection moulding. Alternatively, where compatible base substrate materials, such as alumina are employed, the package leads may be brazed directly to the MCM-D base material and this assembly then processed through the plastic moulding stage. Plastic packaging usually involves lower packaging costs than ceramic packaging and is therefore a preferred option where the level of module integration, thermal dissipation, device stability and compatibility allow.

The above MCM-D packaging techniques all involve greater physical thickness than single chip IC packaging, due to the presence of separate substrate and chip layers.

According to the present invention there is provided a module on board structure in which a microchip module assembly, comprising a microchip module substrate and at least one active semiconductor device mounted on said substrate, is mounted on and connected directly to electrical conductors formed on a surface of a fine line printed circuit board by means of an array of solder bump connections, with said active device between said microchip module substrate and said surface.

Such a structure allows very low profile, low cost assembly and packaging of thin film deposited, MCM-D assemblies directly onto the surface of fine line printed circuit boards. The structure utilises an MCM-D substrate onto which active silicon, GaAs and related devices are assembled by wire bonding or flip chip bonding. This assembly is inverted and mounted on and connected directly to the printed circuit board by an array of solder sphere connections. The mounted assembly may be protected from environmental degradation by filling the space between the inverted MCM-D assembly and the circuit board with a filled epoxy material that has an expansion coefficient closely matched to that of the solder sphere material.

A module on board structure will now be described with reference to the drawing, which shows the structure diagrammatically in cross-section.

Referring to the drawing the MCM-D substrate 1 comprises a silicon, alumina or other suitable base substrate on which is defined the multilayer metallisation and dielectric structure that provides the ground, power and signal routing functions and integrated passive components (not shown). Active devices 2 and 3 are attached to the substrate 1 and interconnected by wire bonding 4 or by flip chip solder bonding 5, the

latter technique being preferred in this case. In either case, the device thickness should be minimised. GaAs devices are conventionally manufactured at 100 to 200 micrometres thickness and are therefore immediately compatible with this structure. Silicon ICs, that are manufactured at 525 micrometres thickness and above, require back lapping to thicknesses of 200 to 300 micrometres in order to be compatible with this approach. The MCM-D substrate base layer will be typically the same thickness as standard silicon IC wafers, i.e. 525 micrometres.

Where flip chip solder bonding 5 is employed, the gap between the chip and the MCM-D substrate is filled with a suitable filled polymeric encapsulent material 6. Such materials are filled with inorganic filler compounds to ensure that the final thermal expansion coefficient is close to that of the solder alloy composition employed in the flip chip solder bonds 5. The underfill material 6 ensures good thermal and power cycling and the absence of voids when the board level assembly is finally encapsulated. The flip chip encapsulent material 6 is applied by a capillary action, infiltration process at a slightly elevated temperature (60 to 100℃) from a series of lines of the uncured encapsulent material dispensed along one or more sides of the flip chip device 2. The underfill material is then cured by a suitable thermal treatment to develop its final properties.

Where wire bonding 4 is employed, film or other adhesive materials 7 may be employed to attach the die to the substrate. The wire bonding is required to be low profile to ensure compatibility with the module on board structure. After wire bonding, polymeric encapsulation of the wires may be employed to provide mechanical protection in subsequent handling operations.

The MCM-D substrate 1 is further provided with larger diameter solder bump connection points 8 to provide the electrical connections to the printed circuit board 9 in the final assembly. These solder bumps 9 will commonly be defined around the perimeter of the module substrate 1, although connections within the substrate area may be employed to advantage in some applications. The solderable metallisation and solder layers for these solder bumps may be applied in the same process steps that are employed to define the solder bumps for the active device attachment. Typical

materials for these layers include solderable CrCuAu multilayer metallisations and 95%Pb-5%Sn solder (wt%). The dimensions and separations of these larger diameter bonds will be determined primarily by the height of the mounted devices 2 and 3 on the MCM-D substrate 1. The bond height must be greater than the mounted component height, i.e. typically greater than 200 micrometres. The bond diameter is likely to be in the range from 100 to 500 micrometres. A proportion of the solder volume required in the final module-to-board connections may be supplied in the substrate bumping process. This may involve a substrate bump thickness between 15 and 125 micrometres. Additional solder volume may be added to the module-to-board connections in the form of discrete solder spheres that are alloyed with the deposited solder layer. Such solder spheres may employ high melting point 90%Pb-10%Sn solder or low melting point eutectic solder as required.

After device assembly to the MCM-D substrate 1 and completion of the underfill and encapsulation processes, the module is functionally tested prior to assembly to the printed circuit board 9.

The fine line printed circuit board 9 to which the MCM-D substrate 1 is attached is provided with a matching array of solderable copper lands and solder bumps as required. The board level solder bumps may be defined using solder plating techniques in which solder is applied over an area larger than the land area and then reflowed to increase the local solder bump height. Alternatively discrete solder spheres may be employed as described earlier. The solderable regions of the copper metallisation on the board are defined by means of a suitably patterned solder resist masking layer.

The prepared substrate module is inverted and soldered onto the bumped printed circuit board 9 using standard surface mounting pick and place and solder reflow equipment. Suitable flux materials may be employed to improve wetting of the solder joints. After solder bonding the flux residues may be removed by appropriate solvent cleaning procedures. The overall solder connection geometries are designed to give a separation between the MCM-D substrate active surface and the circuit board surface of about 400 micrometres.

After solder bonding, the gap between the board and the MCM-D assembly may

be filled, in a similar manner to that employed for the MCM-D flip chip devices 2, with a suitable, filled polymeric encapsulent material 10. As noted earlier, such materials are filled with inorganic filler compounds to ensure that the final thermal expansion coefficient is close to that of the solder alloy composition employed in the flip chip solder bonds themselves. The underfill material 10 ensures good thermal transfer between module 1 and the board 9, and high solder joint reliability under conditions of thermal and power cycling. The reliability enhancement aspect is of particular importance as a result of the mismatch of thermal expansion coefficients between the silicon or alumina MCM-D substrate 1 and the printed circuit board material. The module encapsulent material is also applied by a capillary action, infiltration process at a slightly elevated temperature (60 to 100℃) from a series of lines of the uncured encapsulent material dispensed along one or more sides of the module assembly. The underfill material is then cured by a suitable thermal treatment to develop its final properties. Acceptable reliability is anticipated for such module assemblies up to 15mm on a side between silicon MCM-D substrates and standard, FR4 printed circuit card materials under commercial environmental conditions.

The overall MCM-D module on board structure provides a low profile assembly, with a height equal to the total of the MCM-D substrate thickness and the solder connection height (typically up to 1.0 mm). The area of the assembly is equal to the module substrate area plus the small surrounding miniscus area associated with the incorporation of the underfill material. This then allows the attachment of local heat sink or electrical screening structures (not shown) to the rear of the MCM-D substrate 1. Local screening structures may also be incorporated into the printed circuit board construction below the assembly.

The structure described above also involves the absolute minimum volume of packaging materials and, through the use of the solder connection method, the use of a single mounting and bonding operation. This must therefore lead to a minimal packaging cost for the particular module on board function.

CLAIMS

1. A module on board structure in which a microchip module assembly, comprising a microchip module substrate and at least one active semiconductor device mounted on said substrate, is mounted on and connected directly to electrical conductors formed on a surface of a fine line printed circuit board by means of an array of solder bump connections, with said active device between said microchip module substrate and said surface.

2. A module on board structure in accordance with Claim 1 wherein said active device is mounted on said substrate by flip-chip solder bonding, and spaces left between said device and said substrate after solder bonding are arranged to be substantially filled with a polymer material having a coefficient of thermal expansion substantially matched to that of the solder bonding.

3. A module on board structure in accordance with Claim 1 or Claim 2 wherein the solder bumps are of diameters between 100 and 500 micrometres and the final spacing between the substrate and the surface of the printed circuit board is up to 400 micrometres.

4. A method of making a structure in accordance with Claim 2 wherein solderable metallisation and solder layers for the flip chip bonding and for the solder bump connections are applied to the substrate in the same process steps.

5. A method of making a structure in accordance with Claim 1 wherein solder bumps are defined on connection lands of the printed circuit board by solder plating a larger area than that of each land and then melting the solder plating such that reflow by surface tension increases the height of the solder layer over each respective land.

6. A method of making a structure in accordance with Claim 1 wherein discrete

solder bodies are utilised to add solder volume to the solder bump connections.

7. A module on board structure substantially as hereinbefore described with reference to the accompanying drawing.

Patents Act 1977 Examiner's rep rt t the Comptroller under Section 17 (The Search report) 8	Application number GB 9601609.2
Relevant Technical Fields (i) UK Cl (Ed.O) H1R (RAA, RAB) H1K (KRG, KRX) (ii) Int Cl (Ed.6) H01L, H05K	Search Examiner J DONALDSON Date of completion of Search 26 FEBRUARY 1996
Databases (see below) (i) UK Patent Office collections of GB, EP, WO and US patent specifications. (ii) ONLINE: WPI	Documents considered relevant following a search in respect of Claims :- 1-7

Categories of documents

X:	Document indicating lack of novelty or of inventive step.	P:	Document published on or after the declared priority date but before the filing date of the present application.
Y:	Document indicating lack of inventive step if combined with one or more other documents of the same category.	E:	Patent document published on or after, but with priority date earlier than, the filing date of the present application.
A:	Document indicating technological background and/or state of the art.	&:	Member of the same patent family; corresponding document.

Category	Identity of document and relevant passages		Relevant to claim(s)
X	GB 1137907	(SIGNETICS) see page 2, line 73 - page 3, line 48	1, 6
X	US 4710798	(MARCANTONIO) see column 2, line 18 - column 3, line 23	1, 6

Databases: The UK Patent Office database comprises classified collections of GB, EP, WO and US patent specifications as outlined periodically in the Official Journal (Patents). The on-line databases considered for search are also listed periodically in the Official Journal (Patents)